

What is claimed is:

1. An electroluminescence display device, comprising:
a plurality of display pixels arranged in a matrix within
5 a display pixel region on a substrate, said display pixels having
electroluminescence elements including an emissive layer between
first and second electrodes; wherein
within said display pixel region, a power source line for
supplying power from a power source to said electroluminescence
10 elements is disposed in a grid pattern.
2. The device defined in Claim 1, wherein said power source line
includes main power source lines arranged in plural numbers within
said display pixel region, and at least one bypass power source
15 line extended to intersect and connect said main power lines within
said display pixel region.
3. The device defined in Claim 2, wherein each of said display
pixels further comprises:
20 a first thin film transistor having a gate electrode
connected to a gate line, and a first electrode region connected
to a data line; and
a second thin film transistor having a gate electrode
connected to a second electrode region of said first thin film
25 transistor, a first electrode region connected to one of said main
power source lines, and a second electrode region connected to said
electroluminescence element.
4. The device defined in Claim 3, wherein said first and said

second thin film transistors include active layers composed of poly-silicon.

5. The device defined in Claim 1, wherein said power source line includes main power source lines arranged in plural numbers along the column direction of said matrix within said display pixel region, and at least one bypass power source line extended in the row direction of said matrix within said display pixel region to intersect and connect said main power lines.

6. The device defined in Claim 5, wherein each of said display pixels further comprises:

a first thin film transistor having a gate electrode connected to a gate line, and a first electrode region connected to a data line; and

a second thin film transistor having a gate electrode connected to a second electrode region of said first thin film transistor, a first electrode region connected to one of said main power source line, and a second electrode region connected to said electroluminescence element.

7. The device defined in Claim 6, wherein said first and said second thin film transistors include active layers composed of poly-silicon.

8. The device defined in Claim 5, wherein said main power source lines and said bypass power source line are conductive line integrally formed.

9. The device defined in Claim 5, wherein said main power source lines and said bypass power source line are conductive lines separately formed in different processes.

5 10. The device defined in Claim 9, wherein said bypass power source line is formed in a layer located underneath said main power source lines and separated from said main power source lines by an insulating layer, and is connected to said main power source lines via contact holes.

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11. The device defined in Claim 10, wherein said bypass power source line is formed in a same layer as a gate line.

12. The device defined in Claim 10, wherein said bypass power
15 source line is formed on a gate insulating film, and an interlayer insulating film that separates an active layer of said second thin film transistor and said main power source lines is provided between said bypass power source line and said main power source lines as said insulating layer.

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13. The device defined in Claim 1, wherein said emissive layer is a layer using an organic compound as an emissive material.

14. An electroluminescence display device, comprising:

25 a display pixel region having a plurality of display pixels arranged in a matrix, wherein each of said display pixels includes:
an electroluminescence element having an emissive layer between an anode and a cathode;

a first thin film transistor having a gate electrode

connected to a gate line, and a first electrode region connected to a data line; and

5 a second thin film transistor having a gate electrode connected to a second electrode region of said first thin film transistor, a first electrode region connected to a power source line for supplying power from a power source to said electroluminescence element, and a second electrode region connected to said electroluminescence element; and wherein

10 said power source line is provided in plural numbers along the column direction of said matrix within said display pixel region, and those power source lines that are associated with the display pixels adjacently arranged along the row direction are connected to one another by a bypass power source line extending in the row direction of said matrix.

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15. The device defined in Claim 14, wherein said first and said second thin film transistors include active layers composed of poly-silicon.

20 16. The device defined in Claim 14, wherein said main power source lines and said bypass power source line are conductive line integrally formed.

25 17. The device defined in Claim 14, wherein said main power source lines and said bypass power source line are conductive lines separately formed in different processes.

18. The device defined in Claim 17, wherein said bypass power source line is formed in a layer located underneath said main power

source lines and separated from said main power source lines by an insulating layer, and is connected to said main power source lines via contact holes.

5 19. The device defined in Claim 18, wherein said bypass power source line is formed in a same layer as a gate line.

20. The device defined in Claim 18, wherein said bypass power source line is formed on a gate insulating film, and an interlayer
10 insulating film that separates an active layer of said second thin film transistor and said main power source lines is provided between said bypass power source line and said main power source line as said insulating layer.

15 21. The device defined in Claim 14, wherein said emissive layer is a layer using an organic compound as an emissive material.

22. An emissive display device comprising:

a plurality of display pixels arranged in a matrix within
20 a display pixel region, each of said display pixels having emissive elements including an emissive layer between first and second electrodes; wherein

within said display pixel region, power source line for supplying power from a power source to said emissive elements is
25 disposed in a grid pattern.

23. The device defined in Claim 22, wherein said power source line includes main power source lines arranged in plural numbers along the column direction of said matrix within said display pixel

region, and at least one bypass power source line extended in the row direction of said matrix within said display pixel region to intersect and connect said main power lines.

5 24. The device defined in Claim 23, wherein each of said display pixels further comprises:

a first thin film transistor having a gate electrode connected to a gate line, and a first electrode region connected to a data line; and

10 a second thin film transistor having a gate electrode connected to a second electrode region of said first thin film transistor, a first electrode region connected to one of said main power source lines, and a second electrode region connected to said emissive element.

15 25. The device defined in Claim 24, wherein said first and said second thin film transistors include active layers composed of poly-silicon.

20 26. The device defined in Claim 23, wherein said main power source lines and said bypass power source line are conductive line integrally formed.

25 27. The device defined in Claim 23, wherein said main power source lines and said bypass power source line are conductive lines separately formed in different processes.

28. The device defined in Claim 27, wherein said bypass power source line is formed in a layer located underneath said main power

source lines and separated from said main power source lines by an insulating layer, and is connected to said main power source lines via contact holes.

5 29. The device defined in Claim 28, wherein said bypass power source line is formed in a same layer as a gate line.

30. The device defined in Claim 28, wherein said bypass power source line is formed on a gate insulating film, and an interlayer
10 insulating film that separates an active layer of said second thin film transistor and said main power source lines is provided between said bypass power source line and said main power source lines as said insulating layer.

15 31. The device defined in Claim 22, wherein said emissive layer is a layer using an organic compound as an emissive material.